Investigation of a parasitic-inductance reduction technique for through-hole packaged power devices

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***Abstract* — Parasitic inductance in power electronic circuits can be problematic, giving rise to unwanted overshoots and ringing after switching transients. Whilst the aim is usually to minimize parasitic inductance, the use of through-hole packaged devices with relatively large insertion inductance may be unavoidable, for example due to heat dissipation requirements or device availability. This paper investigates the effectiveness of a technique for reducing the insertion inductance of through-hole packaged devices. The technique is demonstrated with a custom heatsink design for a TO220-packaged Schottky diode. The technique is to exploit the image-plane concept, bringing conductive layers as close as possible to the current loops within the device and its leads. Measurements in a switch-mode GaN test circuit show that the heatsink reduces the parasitic inductance of the diode by 17% when compared to a conventional heatsink.**

Keywords* — *Parasitic Inductance, Image-Plane, Image Current, Pulsed Power, Pulsed Current, Inductance Minimization, Optimal Layout, Heatsink Design

I. Introduction

In switch-mode power electronic circuits, parasitic inductance can be problematic, causing overshoots and ringing on switching events. This in turn can lead to increased electromagnetic interference (EMI) and devices requiring higher voltage ratings than would otherwise be needed. Observing good practice in printed circuit board (PCB) layout [1], in particular minimisation of the enclosed area of high *di/dt* current loops, plays an important role in minimising parasitic inductance. However, this cannot reduce the parasitic inductance introduced by component packaging. The parasitic inductance of through-hole (e.g. TO220, TO247) packaged devices can be of the order of several nanohenries due to the length of the current path along component leads, through bondwires to the die and back; Fig. 1. This level of inductance is significant in high-speed power electronic switching converters such as those employing GaN devices. Surface-mount components often have lower parasitic inductance but cannot always be used, for example due to a device only being available in a through-hole package or due to cooling requirements. The parasitic inductance introduced by through-hole packages is therefore often seen as unavoidable and irreducible. The significant contribution of this work is to apply the well-known image-plane concept [2, 3 (p.391)] in a new way: to a through-hole packaged device via specially-designed heatsink-mounting hardware; and to determine if this has a measurable impact on the parasitic inductance. The results provided allow circuit designers to make an informed decision as to whether the reduction in inductance delivered by this method is large enough to provide sufficient improvement in the performance of their specific circuit to warrant the additional cost of implementation.

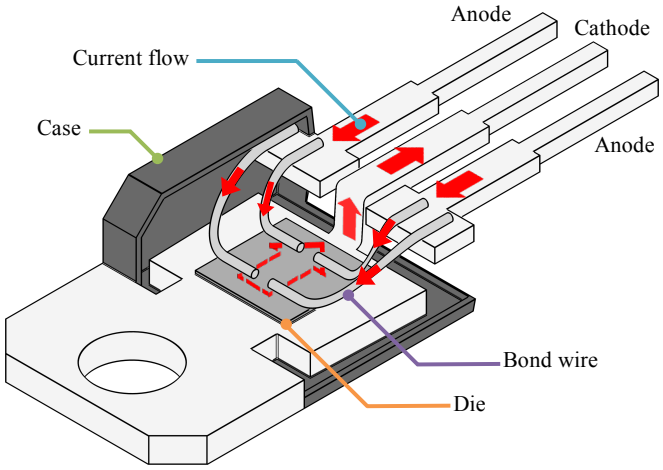

Fig. 1 3D rendering of diode die in a TO220 package showing current pathway when device is forward-biased – along the outer device pins, through the bond wires, vertically down through the die and returning via the device centre pin.

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II. TO220 Parasitic Inductance

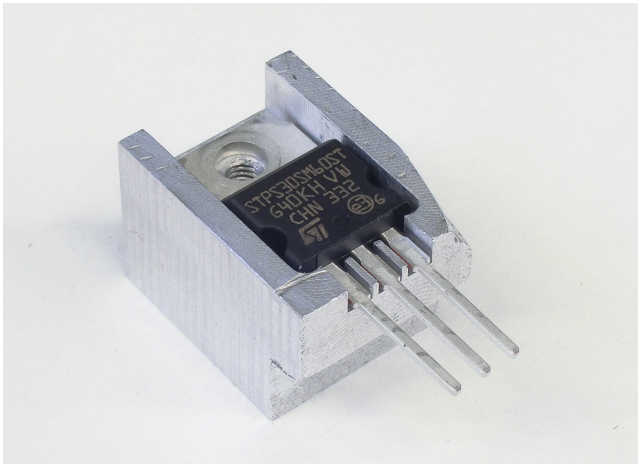
Fig. 1 shows a rendering of a STPS30SM60S diode die inside a TO220 package [4], indicating the current paths when the device is forward biased. The bond wire arrangement shown is an approximation gained from inspection as the manufacturer of this diode does not publish specific details of the device internals.

The parasitic inductance is determined by the specific layout inside the device and is related to the loop area enclosed by the current pathway. As it is not possible to alter the dimensions of this current pathway once the device has been manufactured, it may be expected that the device's parasitic inductance is irreducible. However, the technique presented here places conductive material as close to the device-internal current pathway as possible, in order to allow induced image currents to compensate for magnetic field changes, thereby reducing the inductance. When the current in the device is changing, the magnetic field induced will also be changing. If a metal surface is introduced close to the current pathway, the changing magnetic field will induce a current flow in the metal [2]. This eddy current will itself generate a magnetic field, which will act to oppose the field that originally induced it. This partial cancellation of the magnetic field has the effect of reducing the inductance of the loop for high *di/dt* events, such as during commutation in a hard-switched power electronic circuit.

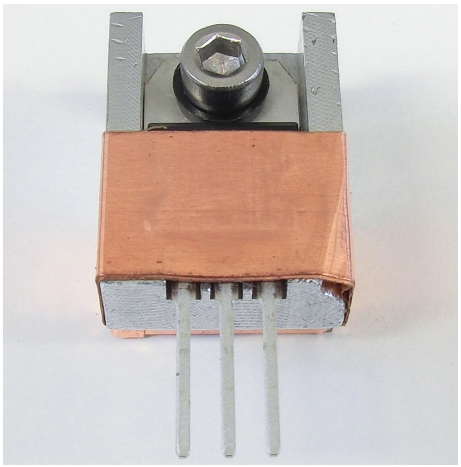
Whilst the image-plane concept is well-known [3], in order to be effective the metal surface must be of sufficient thickness and be located sufficiently close to the current pathway whose inductance is to be reduced, but the package casing imposes a minimum distance. Therefore, it is not immediately obvious that the technique would result in a noticeable reduction in the inductance of a packaged device so the effectiveness of the concept is investigated here experimentally.

III. Heatsink Design

A heatsink adaptor, or mounting block, is designed to bring metal surfaces as close as possible to all parts of the device including its pins, whilst allowing for the TO220's specified manufacturing tolerances. For the nominal package dimensions, the clearance between the metal parts of the device and the mounting block is at least 200 µm. For systems operating at higher voltages than the nominal 12 V used here, the device and mounting block could be encapsulated in electrically isolating material. The mounting block was machined from a solid block of aluminium; Fig. 2*a* shows the diode placed in the mounting block, the device tab being electrically isolated from the block with a thermal pad. For the specific setup used here,



(a)



(b)

Fig. 2 Device placed in custom machined heatsink mounting block.
(a) Without covering copper tape.
(b) With three layers of 35 µm thick copper tape covering topside of device.

this block is in turn mounted onto an off-the-shelf finned aluminium heatsink [5] with additional forced cooling. However, it would be possible to machine the required shapes directly into an aluminium heatsink should this be preferable for the overall system design. Once the device is fixed into the mounting block, it is covered with three layers of 35 µm thick copper tape as shown in Fig. 2*b*, to bring a layer of metal close to the bond wires inside the device. The copper tape does not make electrical contact with any part of the diode, and the heatsink mounting block and heatsink are left "floating", not electrically connected to any circuit node.

IV. Test Circuit

The test circuit employed to investigate the parasitic inductance reduction properties of the proposed heatsink is a simple single-ended inductively loaded switching circuit, as shown in Fig. 3. The circuit is very fast-switching, with an ultra-compact layout to ensure that the critical loop inductance is dominated by the power device under test. The fast nature of the switching ensures that significant ringing will occur on switching transients, allowing the inductance of the Schottky packaging to be inferred.

Transistor Q1 is an EPC2015 Gallium Nitride enhancement-mode High Electron Mobility Transistor (HEMT) from EPC corp. [6] and Schottky diode D1 is a STPS30SM60S from STMicro [4] in a through-hole TO220 package. The load inductance L1 is large in order to maintain a constant current under continuous operation, the series resistor providing volt-second balance to the inductor. The value of the current is controlled by the duty ratio of Q1. The diagram includes relevant parasitic capacitances of Q1 (C_{ds} and C_{dg}), and the lumped parasitic inductance (L_{loop}) of the "critical loop" during transistor turn-off: passing through Q1, D1, and local power supply decoupling capacitors. At Q1 turn-off, this loop inductance will resonate with the transistor capacitances, leading to voltage ringing that can be observed across the drain

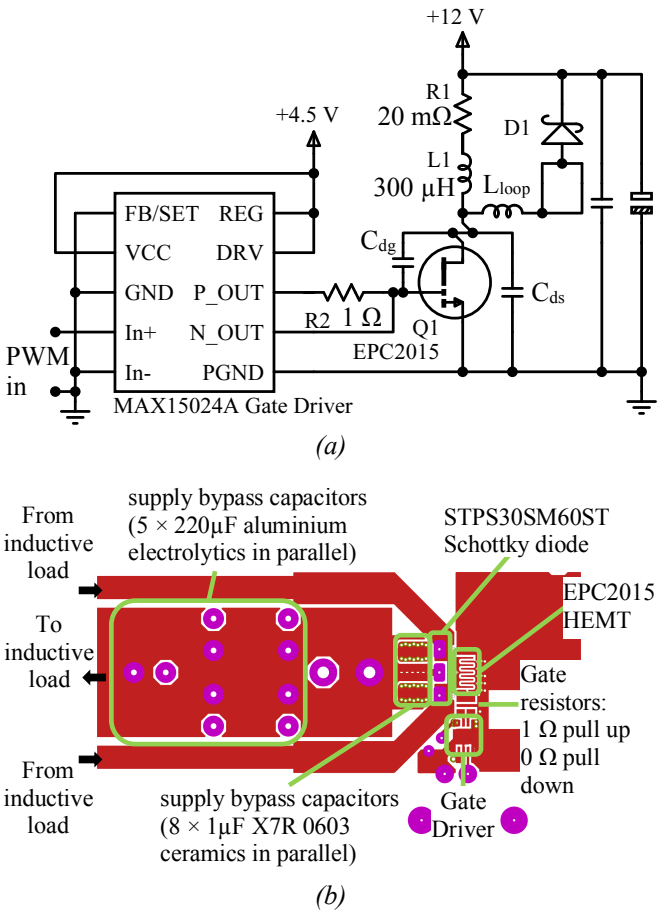


Fig. 3 Inductively-loaded switching test circuit
(a) Simplified schematic including key parasitic components during transistor turn-off event.
(b) Top-side copper pattern of double-sided PCB layout on board with 2oz. copper and 0.5 mm substrate thickness. The bottom side of the board is dedicated to a ground plane.

and source terminals of Q1 (v_{DS}). Careful layout and a thin 0.5 mm substrate mean that the parasitic inductance of the PCB layout is very small, and the loop inductance is dominated by the parasitic inductance of D1.

V. Experimental Results and Discussion

With the Schottky diode mounted to the heatsink via a simple uniform cuboidal aluminium block, the test circuit was operated with a duty cycle of 7.2% to give a load inductor current of 8 A. The ringing observed in v_{DS} during transistor turn-off was recorded. The uniform aluminium mounting block was replaced by

the block and copper tape arrangement shown in Fig. 2*b* and the circuit was then operated under identical conditions with the transistor v_{DS} again being recorded. After the circuit had reached a steady-state temperature, multiple successive waveforms were averaged to improve the signal to noise ratio. The results are shown in Fig. 4; the peak overshoot voltage decreases and the oscillation frequency increases when the machined mounting block is in place, indicating that the loop inductance has been reduced.

Visual inspection of the full switching waveform shows 22 observable cycles of oscillation after the rising edge before the oscillations decay into the noise floor (these cycles are not all shown in Fig. 4 in order to show better the initial oscillation cycles). Therefore, five time-constants of the exponential decay of the oscillation amplitude is approximately equal to 22 oscillation time periods. The circuit damping ratio is therefore given by:

$$\zeta = \frac{1}{2\pi f_0 \tau} \approx \frac{5}{44\pi} = 0.04 \tag{1}$$

where ζ is the damping ratio, τ is the exponential decay time-constant, and f_0 is the circuit natural frequency.

Ignoring this small amount of damping in the circuit, the period of the oscillation observed in v_{DS} is given by the relationship for an L-C resonant tank:

$$T_{osc} = 2\pi\sqrt{L_{loop}C_{oss}} \tag{2}$$

where C_{oss} is the transistor output capacitance given by $C_{ds} + C_{dg}$.

The ratio of loop inductances in the two experiments is therefore given by:

$$\frac{L_{loop,\,improved\ heatsink}}{L_{loop,\,standard\ heatsink}} = \left(\frac{T_{osc,\,improved\ heatsink}}{T_{osc,\,standard\ heatsink}}\right)^2 \tag{3}$$

Substituting the oscillation periods as shown in Fig. 4, it is calculated that the loop inductance is reduced by 17% with the improved heatsink arrangement in place.

It is noted that whilst the results demonstrate that the technique does deliver a noticeable decrease of device parasitic inductance, the benefits to the overall circuit performance in this specific case are small – significant circuit oscillations are still present and other mitigation strategies may be required, such as a dissipative snubber. The benefits delivered by a 17% reduction in device parasitic inductance would of course vary on a circuit-by-circuit basis and in some cases may be considered to be sufficiently beneficial to warrant use of the technique. Use of this technique would increase assembly costs due to the precision machining and device placement required. The results presented in this paper allow system designers to make an informed decision as to whether to use this technique in their system.

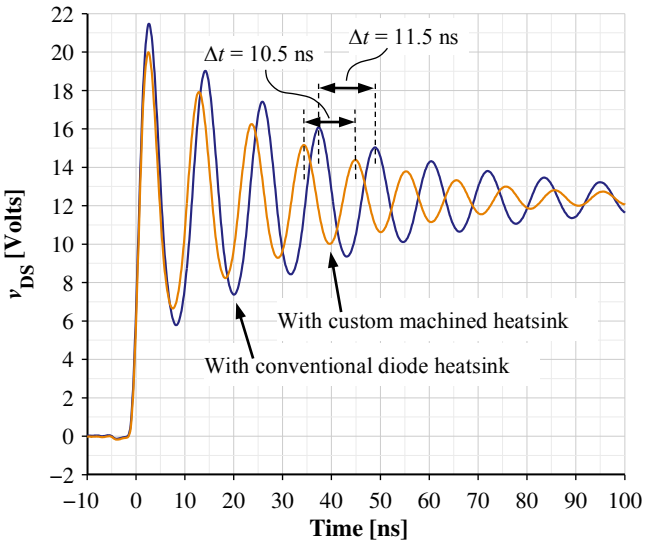


Fig. 4 Measured transistor v_{DS} during turn-off event.

VI. Conclusions

The parasitic inductance of a through-hole component is determined by the device's internal layout such as location of the die, length of bond wires and length of pins. Whilst the circuit designer cannot alter the dimensions of the current loops inside the device, this paper has shown that the parasitic inductance of a through-hole packaged device under dynamic current conditions may still be reduced by the exploitation of the image-plane concept. This paper has

presented the design of a heatsink that employs this technique, bringing a layer of metal as close as possible to the current pathways inside the device. A resulting 17% reduction in the device parasitic inductance has been demonstrated experimentally.

Whilst the concept has been applied to a TO220-packaged diode here, it may be effective with other through-hole packages such as TO247 etc., and indeed in any current-carrying component being operated in a pulsed-current mode with high *di/dt*. The concept does not have to be implemented via a heatsink; any construction method or layout that brings metal surfaces sufficiently close to pulsed-current pathways will have an effect. This may help to maximise performance in niche applications that apply components in unusual ways, i.e. components that are not available in low-inductance packages, because they are not typically used in a dynamic mode.

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